1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the system incorporating the one-chip microcomputer which used the microcomputer with a built-in flash memory.
[0002]
[Description of the Prior Art] Conventionally, the flash memory is already described to the detail by the "Nikkei electronics" (the May, 1992 issue P25 - 62 special edition "magnetic-disk replacement of visible flash plate DRAM") etc.
[0003] And the technique about microcomputer PYUTA (it is hereafter written as a microcomputer) which built in the flash memory as memory for a program is already announced by Hitachi as "H8/538F", and the technique which builds a flash memory in a microcomputer is also already well-known.
[0004] Furthermore, the write-in controller which rewrites the contents of the flash memory is also contained in these "H8/538F" by the program, and possibility of writing a program in the flash memory in a microcomputer where a microcomputer is mounted in a product is also shown.
[0005] On the other hand, in JP,4-170797,A, a microcomputer with a built-in flash memory is used, and the technique which enabled version up of a program, mounted in a product is indicated.
[0006]
[Problem(s) to be Solved by the Invention] However, where the above-mentioned microcomputer is mounted in a product, in order to rewrite the contents of the flash memory in a microcomputer, the hardware write-in controller for rewriting a flash memory by the above-mentioned program control is needed.
[0007] Furthermore, although a product also has circuit version up and circuit version up and a program must be in agreement with the technique indicated by above-mentioned JP,4-170797,A, about that, it is not indicated at all.
[0008] This invention was made in view of the above-mentioned problem, and the place made into the purpose is to suppose that it is possible, mounting version up of a program, even if there was circuit version up while recording the circuit version on the flash memory at the time of production.
[0009]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the system incorporating the one-chip microcomputer of this invention In the system incorporating an one-chip microcomputer the above-mentioned one-chip microcomputer The control means which performs control action according to the program data memorized by a part of nonvolatile memory in which elimination of data and writing are possible, and this nonvolatile memory for every block, A circuit version storage means to memorize the circuit version of the above-mentioned system to a part of above-mentioned nonvolatile memory, At the time of version up of the program memorized by the above-mentioned nonvolatile memory of the above-mentioned system It is characterized by providing the write-in control means which writes the program for version up chosen based on the above-mentioned circuit version memorized by the above-mentioned circuit version storage means in the above-mentioned nonvolatile memory.

[0010]
[Function] The system incorporating the one-chip microcomputer of this invention Elimination of data and writing are possible for nonvolatile memory for every block. A control means performs control action according to the program data memorized by a part of this nonvolatile memory. A circuit version storage means memorizes the circuit version of the above-mentioned system to a part of above-mentioned nonvolatile memory. At the time of version up of the program the write-in control means was remembered to be by the above-mentioned nonvolatile memory of the above-mentioned system, the program for version up chosen based on the above-mentioned circuit version memorized by the above-mentioned circuit version storage means is written in the above-mentioned nonvolatile memory.
[0011]
[Example] Hereafter, the example of this invention is explained with reference to a drawing. Drawing 1 thru/or drawing 3 are drawings showing the internal configuration of the microcomputer for rewriting a flash memory by the program in a detail.
[0012] Drawing 1 is drawing showing the configuration of the 1st example which makes the rewriting basic program of a flash memory hold to ROM first. In this 1st example, the address of a flash memory 1 and ROM2 for boot (it is hereafter written as ROM) is different from each other. M terminal is a terminal for switching which [of the program of ROM2, and the program of a flash memory 1] is performed. That is, in this example, when the reset which is not illustrated on a microcomputer 11 starts, the initialization section 7 determines the address after a reset start, and determines whether to perform the program of a flash memory 1 for whether the program of ROM2 is performed. And this M terminal is connected also to the I/O circuit 3 because which mode or decision is enabled by the program. Furthermore, 12V are an electrical-potential-difference supply terminal for rewriting a flash memory 1. Although the pressure up of 12V may be carried out for a booster circuit from Vcc in preparation for the interior of microcomputer 11a, since a booster circuit needs much area in microcomputer 11a, supplying from the outside like this example is desirable. Moreover, the terminal for enabling actuation [controller / 4 / the exterior to / write-in] other than the above-mentioned 12V is also connected to the write-in controller 4. It may use with an I/O terminal in common, you may connect with the write-in controller 4, and the terminal which enables actuation of this write-in controller 4 is good without a control terminal also as actuation being possible only at a program.
[0013] Next, drawing 2 is drawing showing the configuration of the 2nd example which carried out ROM for boot, and the address of a flash memory in common. In this 2nd example, although both a flash memory 1 and the boot ROM 2 are accessed by power on reset, a selector 10 is switched with M terminal and only one of data is outputted to a data bus 9.
[0014] And drawing 3 is drawing showing the configuration of the 3rd example which does not have ROM for boot. In this 3rd example, if mounted in a product, data cannot be written in a flash memory 1, but if the plug ram for boot at least later mentioned before mounting is written in by the ROM writer, it will enable after mounting of a product to rewrite the program in a flash memory 1 using the program concerned.
[0015] Here, drawing 4 is drawing showing an example of the address map of the flash memory 1 of the microcomputer 11 mentioned above. The description of a flash memory 1 is to make data elimination and data writing, i.e., rewriting, for every block. And it has classified into the block to block 0 - block 7 (it is hereafter written as B0-B7) in the example shown in this drawing. In addition, although the memory space within each block serves as 8K, 1K, and 512,256,128 bytes and various values, it is good also as constant value, such as 8 etc. K bytes.
[0016] Although explanation is hereafter continued about the example using a flash memory 1, when using the nonvolatile memory of a block rewriting method, of course, it is effective also except flash memory 1. Furthermore, in the following explanation, the microcomputer 11 of the 1st thru/or the 3rd example shown in above-mentioned drawing 1 thru/or drawing 3 will be called microcomputer 11a, microcomputer 11b, and microcomputer 11c, respectively.
[0017] Drawing 5 is a flow chart which shows the actuation for writing data in all blocks of a flash memory 1. Although this program is surely required of the microcomputers 11a and 11b with ROM2 in ROM2, this program cannot be used in microcomputer 11c. This is for also rewriting the program for

rewriting gradually in microcomputer 11c. In addition, in microcomputer 11a and b, this program is performed after reset.
[0018] Now, if this program is performed, M terminal (in the case [Microcomputer 11] of a and b), and 12V and other control terminals will be checked first, and it will judge whether it can write in or not (step S101). And in the case of write-in impossible, an abnormality signal is sent to program transfer equipment 19, and it is completed (steps S111 and S112).
[0019] On the other hand, when it can write in, the program (B0) of the beginning of a flash memory 1 is specified continuously (step S102). And a data demand signal is outputted to program transfer equipment 19 (step S103). Then, since program data are transmitted from program transfer equipment 19, it stores in the storage region of RAM5 where this data was received and it was beforehand decided in the microcomputer (step S104). Then, after eliminating the block of a flash memory 1 by which current assignment is carried out (step S105), the data stored in the above RAM 5 are written in the block with which the flash memory 1 is specified (step S106). When verifying the contents of RAM5 and the flash memory 1 (step S107), incrementing designated block if that result is "O.K.", checking whether it has ended to the last block and having not finished to the last block after this data is written in, the above-mentioned step is repeated (steps S108 and S109). And when it finishes to the last block, a terminate signal is outputted to program transfer equipment 19 (step S110), and program writing is ended (step S112). Furthermore, when the result of the verification in the above-mentioned step S107 is "NG", an abnormality signal is sent to program transfer equipment 19, and this program is ended (steps S111 and S112).
[0020] Next, drawing 6 is a flow chart which shows actuation of the program "specific block rewriting" which rewrites only the specific block of a flash memory 1. Although this program is written in in ROM2 or a flash memory 1 by microcomputer 11a and b, in microcomputer 11c, it is written in by the ROM writer at the time of a microcomputer simple substance. In this case, it shall write in B0. In addition, when there is no ROM2 at microcomputer 11a and b, it is written in one flash memoryB0. Furthermore, this program is performed by carrying out a subroutine call by the subroutine "a checker communication link" later mentioned from program transfer equipment 19.
[0021] If this program is performed, when it judges whether the write mode is specified first (step S201) and the write mode is specified, it judges continuously whether designated block is "0" (step S202). And when designated block is not "0", the data of designated block are eliminated (step S203), designated block of writing (step S204), RAM5, and a flash memory 1 is verified for the data of RAM5 to designated block (step S205), and when the result is "O.K.", the return of the terminate signal is sent and (step S206) carried out to program transfer equipment 19 (step 208).
[0022] On the other hand, the case where it is not a write mode at the above-mentioned step S201, when designated block is "0" at the above-mentioned step S202, or when the result of having verified designated block of RAM5 and the FURAYUSHU memory 1 at the above-mentioned step S205 is "NG", an abnormality signal is sent to program transfer equipment 19 (step S207), and this program is ended (step S209).
[0023] Thus, a different point of this program "specific block rewriting" and the program "program writing" previously shown in drawing 5 is for this program to rewrite only the block specified before being called. However, B0 in which this program is stored has applied prohibition to the appearance which is not rewritten. This is because the program currently performed will disappear and it will become rewriting impossible, when Assignment B is eliminated if it is going to rewrite this block. Moreover, after rewriting termination, it has ended by the return so that it can return to a subroutine "a checker communication link." In addition, although "specific block rewriting" was explained as an example written in B0, it is natural here. [of it being possible at other blocks]
[0024] Next, drawing 7 is the block diagram showing the configuration of the camera which applied the system which has the one chip microcomputer of this invention. In this drawing, the one chip microcomputer 11 for performing the sequence of a camera and control has the flash memory 1 rewritable by program control. Furthermore, the connector 15 for an external communication link for connecting the equipment which writes in the flash memory write-in control terminal 14 for connecting the AF circuit 12 which measures the distance to a photographic subject, the AE circuit 13 which measures the brightness of a photographic subject, and program transfer equipment 19, and the

adjustment machine of a camera and the data for ROM correction, and the terminal for flash memory write-in control and the stroboscope 16 which performs stroboscope charge and luminescence are connected to this microcomputer 11.
[0025] In this flash memory write-in control terminal 14, M terminal mentioned above and the terminal of 12V and others are included. In addition, a common connector is sufficient as this flash memory write-in control terminal 14 and the connector 15 for an external communication link.
[0026] In addition, motor ML which drives a focal lens through Motor Driver 17 for [various] motorised one on the above-mentioned microcomputer 11 Magnet Mg for closing the motor MZ which drives a zoom lens, the motor MW which performs winding rewinding [of a film], the motor MS which drives a shutter, and the above-mentioned shutter It connects.
[0027] Moreover, switch SL which detects the initial valve position of a focal lens on a microcomputer 11 Switch SS which detects the initial valve position of the photo interrupter PIL which detects the amount of unit drives of a focal lens (location), the photo interrupter PIZ which detects the location of a zoom lens, the photograph reflector PR which detects the perforation of a film, and a shutter It connects.
[0028] Furthermore, the various switches of the power switch 18, the first (1st) release switch 21, and the second (2nd) release switch 22 are connected to the above-mentioned microcomputer 11. In addition, 1st release switch 21 and 2nd release switch 22 constitute the two-step switch, and 2nd release switch 22 is turned on with the 21 or 2nd step of release switch in the 1st step.
[0029] Hereafter, actuation of this camera is explained with reference to the flow chart of drawing 8 . If the cell which is not illustrated is fed into a camera, the port and others of a microcomputer 11 will be initialized (step S301). Then, a CHECK terminal checks high level"H" or a low level "L", and the subroutine "a checker communication link" which will be later mentioned if it is "L" is performed (steps S302 and S303).
[0030] And when the power switch 18 is ON, a camera stands by until 1st release switch 21 is pushed, and when the switch 21 concerned is pushed, it performs the subroutine "release processing" mentioned later. Furthermore, when the power switch 18 is OFF, it will be in a standby condition until the power switch 18 is turned on. Since this invention has little relation, other detailed processings omit explanation (steps S304, S305, and S306).
[0031] Next, with reference to the flow chart of drawing 9 , actuation of the above-mentioned subroutine "a checker communication link" is explained. In addition, since it is already indicated about this subroutine "a checker communication link" by JP,2-941,A by the applicant for this patent, detailed explanation is omitted and only that concept explains it here.
[0032] A synchronizing signal and the clock for serial communication are outputted outside from a microcomputer 11 (step S401,402), and data are received from the exterior (step S403). Here, it will be termination if there are no data. When data are received, after judging the mode of memory (step S404), if it is a Read mode, the semantics of the data will be decoded, and the data of the address with which it was specified in the microcomputer 11 are read (step S405). Then, data are outputted to a serial line (step S406), and it escapes from this routine.
[0033] Check data are checked when the mode of the above-mentioned memory is a write mode (step S407) (step S408). And data are written in the address specified when the result was good (step S409). Moreover, when it is in subroutine call mode (step S410), check data are checked (step S408), the subroutine of the address specified when the result was good is called (step S412), and the subroutine of the specified address is performed.
[0034] Furthermore, when it is the continuation communicate mode which performs only the communication link with the exterior, it judges whether it is in (step S413), then the continuation communicate mode (step S414). And "a checker communication link" is performed after performing a checker communication link again (step S415) until a CHECK terminal becomes "H", when it is not among the continuation communicate mode (step S416). And when it is in off mode which stops a continuation communication link, it judges whether it is among (step S417) and continuous mode (step S418). And if it is among continuous mode, it is 1 level **** (step S419) about a stack pointer. "Specific block rewriting" program execution mentioned above, adjustment of a camera mentioned later can be performed using this checker communication link.

[0035] Next, with reference to the flow chart of drawing 10 , actuation of the subroutine "release processing" performed with the above-mentioned camera is explained to a detail. Activation of this program performs ranging which performs the photometry which measures the brightness of a photographic subject first (step S501), and measures the distance to a photographic subject continuously (step S502). Furthermore, by AE operation, the data in the fresh memory for amending the variation in the photometry value of camera each based on the above-mentioned photometry value are used, it amends to the photometry value of normal (step S503), and AF operation amends the amount of drives of a focal lens to a proper value for every camera using the data in the flash memory 1 which amends the variation in camera each (step S504).
[0036] Then, 2nd release switch 22 is checked, it stands by until it will be turned on, if off, and processing will be ended if 1st release switch 21 becomes off into [off] 2nd release switch 22 (step S505,506). And if 2nd release switch 22 is turned on, a focal lens will be driven by lens drive, a shutter will be opened, and deed processing will be ended for film winding (steps S507-S510).
[0037] Here, drawing 11 is an image Fig. for adjusting each variation of the above-mentioned camera, and as shown in this drawing, the camera 33 is connected to the regulator 32 through the external communication link connector. And the measuring instrument or the reference-value output unit 31 is also connected to the regulator 32. Furthermore, if it is AF adjustment, a lightwave signal will be outputted to measurement distance considerable the bottom, and if it is AE adjustment, the specific brightness for adjustment will be outputted.
[0038] Next, drawing 12 is the image Fig. of production-adjustment Rhine of the above-mentioned camera. In drawing 12 (a), a program is first transmitted to the flash memory 1 of the microcomputer 11 in a camera with program transfer equipment 19, and the amendment data adjusted at the end through AF adjustment, AE adjustment, etc. are written in a flash memory 1 with adjustment value write-in equipment. The amendment data to this adjustment termination are stored temporarily at RAM5 in the microcomputer mentioned later, and, finally are written in at once. In this case, if a work from which it moves to the next adjustment is carried out after making the microcomputer 11 in a camera standby, even if it continues adjustment in the condition of having put into the cell, to a camera or extracts a cell, it can back up, if it is a short time in an internal filter capacitor, and the data of RAM5 in a microcomputer 11 will not break.
[0039] It is the image Fig. of adjustment Rhine in case there is a possibility that the data of RAM5 in a microcomputer 11 may break, and after adjustment starts, the regulator is connected on-line, and drawing 12 (b) sucks up amendment data on-line, and, finally writes amendment data in a flash memory 1. If it does in this way, even if the contents of RAM5 break, amendment data can be written in for every one camera.
[0040] Next, drawing 13 is a flow chart which shows the program by the side of the transfer equipment 19 in the case of transmitting a program with the above-mentioned program transfer equipment 19 after assembly to a product, and corresponds to the above-mentioned microcomputer 11a and b.
[0041] Activation of this program "a program transfer" sets the circuit version of this product first (step S601). The reason for setting this circuit version is that it can perform version up of a program easily by replacing a program even if a program bug is discovered behind if it is the microcomputer 11 which has a flash memory 1. However, there are many things for which the circuit of a product may also have fault and a circuit is also upgraded from the time of production initiation. Then, even when a bug is discovered, the version up which could not replace a program simply but was doubled with the circuit is needed. Therefore, it is necessary to make a part of flash memory 1 in the microcomputer 11 of a product memorize the data of a circuit version. This is stated to the detail at Japanese Patent Application No. 5-51752.
[0042] now, the terminal M after setting a circuit version in this way -- "H", i.e., a program write mode, -- setting up (step S602) -- further -- 12V are supplied, and if there is need, other control terminals will also be set as a write mode (step S603). If reset is applied to a microcomputer 11 (step S604), since the above-mentioned program "program writing" in ROM2 in a product will be performed, data are transmitted according to directions and data are written in a flash memory 1 (step S605).
[0043] Next, drawing 14 is a flow chart which shows the data write-in example to the flash memory 1

at the time of performing the above-mentioned program "specific block rewriting" by microcomputer 11a, and b and c. It is necessary to write in this program by the ROM writer at the time of a microcomputer item, and in microcomputer 11c, when this program does not exist into ROM2 at microcomputer 11a and b, it is necessary to write in this program beforehand using a ROM writer or a subroutine "a program transfer."

[0044] Now, if this program is performed, the circuit version of a product will be set first (step S701), the CHECK terminal of a product will be set to "L" (step S702), and reset will be applied to a microcomputer 11 (step S703). Then, since actuation of a subroutine "a checker communication link" is started, it is set as the continuation communicate mode and enables it to do the following activities (step S704).

[0045] 12V are supplied first, and the write-in control terminal of need owner **** and others also becomes a write mode, and carries out an appearance set (step S705). Then, it writes in 1 block of programs at a time from the one following flash memoryB1 with a program "the program transfer 2." And a program will be ended if the writing of a block of all the programs for camera actuation is completed (step S 706-711). In addition, it is not necessary to write in B7 which is an adjustment data area.

[0046] Here, drawing 15 is an example which writes a program in a flash memory 1 in the state of a microcomputer item. A microcomputer 11 is set to PROM writer 41, and the control section 42 controls writing of a program on a microcomputer 11.

[0047] Furthermore, drawing 16 is a flow chart which shows write-in actuation for the program of the control section 42. Drawing 16 (a) is a flow chart which shows the sequence in the case of loading only a subroutine "specific block rewriting", and after it mounts the microcomputer mentioned later in this case in a camera, it writes the program for camera control in a flash memory 1 by the technique shown in drawing 23 (step S 801-803). And drawing 16 (b) is a flow chart which shows the sequence in the case of also writing in the program for camera control beforehand. In this case, since it is not necessary to write a program in a flash memory 1 after mounting a microcomputer 11 in a camera, a program transfer of the first step shown in drawing 21 is omitted (step S 811-813).

[0048] Next, with reference to drawing 17 , the zoom focus amendment in AF adjustment is explained. In addition, since this is described in detail by JP,1-201634,A (U.S. Pat. No. 4914464 number), it explains briefly here.

[0049] The axis of abscissa of this drawing is the value (wideness and 40H call [0H]) of a zoom encoder, and an axis of ordinate is the focal lens delivery pulse correction value from the criteria focus location at the time of the focal infinity in each zoom location. And every zoom encoder 10H memorizes as correction value D0-D4 at nonvolatile memory. At the time of actual camera use, if the above-mentioned correction value is applied to the amount of focal lens criteria delivery, it will be changed into the amount of delivery of the focal lens which amended the variation in camera each. In addition, this operation is used in the subroutine "AF operation" of drawing 10 .
 [0050] Next, drawing 19 is a flow chart which shows an example of the program of AF regulator in the case of performing the above-mentioned zoom focus amendment at the time of using the flash memory 1 in the microcomputer 11 of this invention for amendment data.

[0051] if this program is performed -- first -- i -- initializing (step S901) -- a zoom -- being wide (0H) -- it moves (step S902). Then, a focal lens is moved to the criteria location of infinity (step S903). Here, the lens is referring to the chart of infinity, measures the amount of defocusing of a lens with a focal measuring instrument, changes this amount of defocusing into the delivery pulse value of a lens, and assigns this changed value to D (i). And this D (i) is stored in RAM5 in a microcomputer 11 (step S904,905). Although you may substitute for a flash memory 1 directly, it is more rational to write in a flash memory 1 at once from there being few counts of a guarantee, by rewriting the flash memory 1 in that a write time starts or a microcomputer 11, after other the adjustments of all finish.

[0052] the following and a zoom -- an encoder value -- 10 -- it moves every [H] and the amendment data which repeat the above-mentioned actuation and are substituted for D0-D4 are determined (steps S910-S912). Then, after returning a zoom widely (step S913) and setting a ranging value to infinity, an actual subroutine "AF operation" is performed (step S914), the operation using the above-mentioned correction value is performed, a focal lens is driven based on the result (step S915), and a

focus is checked (step S915). And if the result is good, all actuation will be ended (step S917), and if bad, it will consider as bad alignment (step S918).
[0053] Next, drawing 18 is drawing showing an example using nonvolatile memory of photometry value amendment. In addition, since it is already opened to the public by JP,62-25733,A about this, it explains briefly here.
[0054] In this drawing, nonvolatile memory 20 is made to memorize the error of the value and certified value which measured the strength of the light by the brightness of criteria, and the value which measured the strength of the light at the time of camera use is amended by the photometry value of normal based on the above-mentioned error value (correction value) within the subroutine "AE operation" shown in drawing 10 .
[0055] Next, drawing 20 is a program by the side of the regulator for creating the above-mentioned photometry amendment data which are a part of AE adjustment in a flash memory 1. Activation of this program makes the brightness of a brightness regulator the predetermined value for adjustment first (step S1001). Then, an error (usually 0) general to FCV is set (step S1002). This FCV is a variable which substitutes the data for correction value written in a flash memory 1. Then, a subroutine "a photometry" is performed (step S1003). Then, since "0" is contained in correction value, since error part deltavalve flow coefficient to a certified value is outputted, a photometry value performs a subroutine "AE operation" and calculates deltavalve flow coefficient (step S1004). Therefore, a photometry value can be amended if this deltavalve flow coefficient is substituted for Above FCV (step S1005). Then, a subroutine "a photometry" is performed again (step S1006), a subroutine "AE operation" is performed after that using Above FCV (step S1007), and it checks whether it is amended correctly (step S1008). And when the result is "O.K.", it ends (step S1009), and in the case of "NG", it is made into bad alignment (step S1010).
[0056] Next, drawing 21 is an example of the address map of the flash memory 1 in case there is no program "specific block writing" into microcomputer 11c or ROM2. In this drawing, a program "specific block writing" may arrange to B0, and you may write the subroutine which is absolutely bug-free in this block. Since this B0 is not eliminable from there being a "specific block write-in" program, 11 should just devise placing first the instruction jumped to the following block etc. with a microcomputer which is started from the address "0000" by power on reset. Moreover, what is necessary is to consider that it is not only eliminable, when it is chosen as the location which stores a "specific block write-in" program except this B0. Furthermore, B1 - B6 are the programs for camera control, and made B7 the data area for adjustment data (correction value) here. It is user-friendly when the "circuit version" data mentioned above in the adjustment data area are also stored. Moreover, with this microcomputer 11, the point was made into RAM area from the address "9000."
[0057] Here, in adjustment by drawing 19 and drawing 20 , adjustment using the program at the time of actual camera use is performed. Although an actual subroutine "AF operation" and "AE operation" use the data in a flash memory 1 as correction value, it is larger for a merit for a flash memory 1 not to rewrite as mentioned above at the time of adjustment.
[0058] Then, it is possible to change to address "8700"[of a flash memory 1] - "877F" at the time of adjustment, and to substitute for it using address "9000"[of RAM5] - "907F." That is, if it replaces with a flash memory 1 by a certain approach at the time of adjustment and adjusts using RAM5, what is necessary will be just to transmit RAM5 to a flash memory 1, after all adjustments finish.
[0059] Four kinds are explained about the example of the approach of replacing with a flash memory 1 and substituting for RAM5 hereafter. Drawing 22 is drawing showing the technique of substituting the hardware in a microcomputer 11 for RAM5 first. In this drawing, address buses A8-A15 are supervised, and when A8-A15 are [signals] "H" during "87" and adjustment, it is the method changed into "90." And the address bus after modification is connected only to a flash memory and RAM. In addition, even if it uses the signal for adjustment also [port], it is good also as a register in a microcomputer etc.
[0060] Next, drawing 23 is drawing showing the technique of moving the data of a flash memory 1 to RAM5 once, and using the data on RAM5 as amendment data. Here, as the flow chart of drawing 8 is shown in drawing 23 (b), it is used, changing. First, the data of a flash memory (address "8700"- "877F") 1 are transmitted to RAM (address "9000"- "907F")5 after power-on, and it is henceforth

made after that the step of a subroutine "a checker communication link." In this case, since the data with which it memorizes by "AF operation" and "AE operation" in the storage region of RAM5 also at the time of actual camera use are used as correction value, it is good only by writing correction value in RAM5 at the time of adjustment (step S 1101-1104).
[0061] And drawing 24 is drawing showing the technique in which after "00H(a)" and adjustment writes "A5H (b)" in front of adjustment at the predetermined address (for example, address "8700") of a flash memory 1. By "AE operation" and "AF operation", all judged parts whenever it uses the value of a flash memory 1, as beforehand shown in a program at drawing 24 (c) are contained. That is, if it is "00", the data of RAM5 will be read, and if it is "A5", the data of a flash memory 1 will be read. Therefore, 8 bits of low order of the address of a flash memory 1 and RAM5 correspond by 1 to 1.
[0062] Furthermore, drawing 25 is drawing showing the technique of rewriting a program adjustment before and the adjustment back, and "AFC1"- "AEC2" is a label in which the address of a flash memory 1 is shown in this drawing. However, the address of RAM is set up and linked at the time of adjustment. The program for adjustment is "CAMERA ADJ." After adjustment links and sets the address of the flash memory of normal. The program of normal is "CAMERA ADJ." And after adjustment links and sets the address of the flash memory 1 of normal. The program of normal is "CAMERA USE."
[0063] Next, drawing 26 is a flow chart which shows the program of program transfer equipment 19. If this program is performed, before camera adjustment, "CAMERA ADJ" will be transmitted to a flash memory 1 (step S 1301, 1302, 1305), and the amendment data after adjustment and "CAMERA USE" will be transmitted to a flash memory 1 after camera adjustment termination (step S 1301, 1303, 1034, 1305). In addition, although the example which changes only label data here was shown, even if it completely changes the program for adjustment, and the program after completion, of course, this approach can be used. Furthermore, it becomes effective technique when the capacity of the program for adjustment is very mostly needed.
[0064] Next, drawing 27 is the flow chart of the adjustment value write-in equipment which writes the amendment data totaled a RAM5 top or on-line after adjustment termination in the B7 a flash memory 1 and here. By the case where the amendment data which remain on RAM5 of a microcomputer are written in, drawing 27 (a) increments the count of rewriting of the flash memory 1 on B7 first. Next, it is set as a write mode, B7 is specified, and a program "specific block rewriting" is performed (steps S1401-S1405).
[0065] And drawing 27 (b) is the same as drawing 27 (a) except transmitting the data totaled on-line to RAM5 in a microcomputer 11 by the case where the data totaled on-line are written in (step S 1411-1417).
[0066] Furthermore, by the case where all the area of the flash memory 1 which used Microcomputers a and b is rewritten, drawing 27 (c) reads the amended data on RAM5 first, and it prepares them so that it can write in B7. Next, the count of rewriting of a flash memory 1 is incremented, and it is set as a write mode. Next, all the area of a flash memory 1 is rewritten using a "program write-in" program (steps S1421-S1425). In this case, the program "specific block rewriting" is unnecessary.
[0067] Moreover, drawing 28 is a flow chart which shows the program by the side of the program transfer equipment 19 which upgrades a program to a repair store or works (at the time [Middle] of a production change-over or repair), when a bug is discovered by the program.
[0068] Activation of this program judges whether correction of only a reader is sufficient in the circuit version which is in B7 first. And in the case of NG, version up of a circuit is directed (step S1503). On the other hand, in O.K., the adjustment value (data for amendment) of B7 is read (step S1504). Then, the count of rewriting of a flash memory 1 is incremented (step S1505). And it sets so that the version up program suitable for a circuit version can be chosen and transmitted (step S1506). Furthermore, a microcomputer 11 is set to a program write mode (step S1507), and a program is transmitted and written in (step S1508).
[0069]
[Effect of the Invention] The system incorporating the one-chip microcomputer made possible, mounting version up of a program even if there was circuit version up while recording the circuit

version on the flash memory at the time of production according to this invention as explained in full detail above can be offered.

[Translation done.]

CLAIMS

[Claim(s)]
[Claim 1] The system incorporating an one-chip microcomputer characterized by providing the following The above-mentioned one-chip microcomputer is nonvolatile memory in which elimination of data and writing are possible for every block. The control means which performs control action according to the program data memorized by a part of this nonvolatile memory A circuit version storage means to memorize the circuit version of the above-mentioned system to a part of above-mentioned nonvolatile memory At the time of version up of the program memorized by the above-mentioned nonvolatile memory of the above-mentioned system, it is the write-in control means which writes the program for version up chosen based on the above-mentioned circuit version memorized by the above-mentioned circuit version storage means in the above-mentioned nonvolatile memory.

[Translation done.]